REMARKS/ARGUMENTS

In the Office Action mailed September 16, 2008, claims 1-7 were rejected. In response, Applicants hereby request reconsideration of the application in view of the proposed amendments and the below-provided remarks. Applicants submit that the proposed amendments place the present application in condition for allowance or in better condition for appeal.

For reference, proposed amendments are presented to cancel claims 1-7 and add new claims 8-19. In particular, the proposed amendment for claim 8 recites means for performing discrete linear transform and inverse discrete linear transform operations, as well as a control circuit to selectively activate at least one of a plurality of filtering modules. This proposed amendment is supported, for example, by the subject matter described in the original language of claim 1, which is canceled, as well as the subject matter described at page 4, lines 15-24, of the specification. The proposed amendment for claim 9 recites the control circuit selectively activates the at least one of the plurality of filtering modules based on a predicted maximum frequency (kwpred) and a quantization step (Q). This proposed amendment is supported, for example, by the subject matter described at page 10, lines 10-17, of the specification. The proposed amendment for claim 10 recites first and second odd filtering modules (FILo1 and FILo2). This proposed amendment is supported, for example, by the subject matter described in the original language of claim 2, which is canceled. The proposed amendments for claims 11 and 12 recite a discrete transform means and an even filtering module (FILe) for first, or first and second, even transformed data values. These proposed amendments are supported, for example, by the subject matter described in the original language of claim 2, which is canceled. The proposed amendment for claim 13 recites transforming first and second halves in succession at double frequency. This proposed amendment is supported, for example, by the subject matter described in the original language of claim 2, which is canceled, as well as the subject matter described at page 10, lines 10-17, of the specification. The proposed amendments for claims 14 and 15 are supported, for example, by the original language of claim 3, which is canceled.

The proposed amendments for claims 16-19 are respectively supported, for example, by the original language of claims 4-7, which are canceled.

Claim Rejections under 35 U.S.C. 112

Claims 1-7 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, claim 1 was rejected because lines 3 and 4 are grammatically incorrect. Claim 1 was also rejected because it is unclear as to what is being referenced by the "having" phrase of line 6. Claim 1 was also rejected because lines 7 and 8 are mis-descriptive because the set of transformed data is filtered. Additionally, claim 2 was rejected because lines 1 and 2 recite the phrase "the discrete transform means (DCTN)," without proper antecedent basis.

Applicants submit that the proposed amendments herein cancel claims 1-7. Hence, the rejections of claims 1-7 are rendered moot.

Claim Rejections under 35 U.S.C. 102

Claims 1 and 3-7 were rejected under 35 U.S.C. 102(a) as being anticipated by Applicants' own admission. However, Applicants submit that the proposed amendments herein cancel claims 1-7. Hence, the rejections of claims 1-7 are rendered moot.

New Claims

Applicants respectfully assert claims 8-19 are patentable over the prior art relied on in the Office Action. Specifically, the claims of the present application recite limitations which are not shown to be in the prior art relied on in the Office Action.

Claim 8 recites "a control circuit coupled to the means for performing the discrete linear transform and the inverse discrete linear transform, wherein the control circuit is configured to selectively activate at least one of a plurality of filtering modules, wherein the plurality of filtering modules comprises at least one odd filtering module to filter at least one of the odd transformed data values and at least one even filtering module to filter at least one of the even transformed data values" (emphasis added).

In contrast, the prior art relied on in the Office Action does not disclose a control circuit which selectively activates filtering modules, as recited in the claim. While some details of a conventional implementation of a filtering sequence are discussed in the present application, the present application does not describe any modular filtering sequences. More specifically, the present application does not describe a conventional implementation which uses a control circuit to selectively activate one or more filtering modules.

Additionally, the present application does not describe a conventional implementation which uses odd and even filtering modules. Rather, the conventional implementation described in the present application merely uses separate modules for different segments, u and v, without separating odd and even data values within a particular segment. The conventional implementation also uses a combined module for the concatenated segment data, w, which is a combination of all of the odd and even data values of both input segments. Similarly, the description of the conventional implementation recognizes that the inverse discrete transform module processes both odd and even transformed data from both segments. Hence, none of the modules of the conventional implementation separately processes odd and even data.

Furthermore, although the Office Action attempts to construe the individual logic gates which might be used in the conventional implementation as separately processing odd and even data values, the Office Action does not provide support for this assertion. Moreover, even if individual gates were used to process odd and even data values in the conventional implementation described in the present application, there is no description of the conventional implementation using control circuit to selectively activate odd and even filtering modules. In other words, the present application does not describe a conventional implementation in which a control circuit might activate individual logic gates to process odd data values independently of activating separate logic gates to process even data values. Rather, from the description of the conventional implementation referenced in the present application, the operational blocks shown in Fig. 2 of the present application do not distinguish between odd and even data values. Hence, there is no way for the operational blocks of the conventional implementation described in the present application to selectively operate individual logic gates, or

groups of logic gates, in order to filter odd and even data values. Therefore, the prior art relied on in the Office Action does not describe a control circuit to selectively activate odd and even filtering modules to filter odd and even transformed data values.

For the reasons presented above, the prior art does not disclose all of the limitations of the claim because the prior art does not disclose control circuit to selectively activate odd and even filtering modules to filter odd and even transformed data values, as recited in the claim. Accordingly, Applicants respectfully assert claim 8 is patentable over the prior art because the prior art does not disclose all of the limitations of the claim.

Given that claims 9-19 depend from and incorporate all of the limitations of independent claim 8, Applicants respectfully assert claims 9-19 are allowable based on an allowable base claim. Additionally, each of claims 9-19 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the proposed amendments and the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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